REMARKS

Applicants appreciate the Examiner's thorough examination of the present application as evidenced by the Office Action of July 12, 2005 (hereinafter "Office Action"). In response, Applicants respectfully submit that the cited references do not disclose or suggest all of the recitations of the independent claims. Accordingly, Applicants submit that all pending claims are in condition for allowance. Favorable reconsideration of all pending claims is respectfully requested for at least the reasons discussed hereafter.

Independent Claims 1, 14, 19 are Patentable

Independent Claims 1, 14, and 19 stand rejected under 35 U.S.C. §102(e) as being anticipated by U. S. Patent No. 6,516,422 to Doblar et al. (hereinafter "Doblar").

Independent Claim 1 is directed to a clock distribution circuit that comprises both a first and a second clock circuit that are each responsive to an error signal as indicated by the recitations of Claim 1 reproduced in part below:

> a first clock circuit that is configured to generate a first clock signal responsive to an error signal;
> a second clock circuit that is configured to generate a second clock signal responsive to the error signal; (emphasis added)
> ...

Independent Claim 14 is directed to method for distributing a clock signal in which both a first and a second clock signal are each generated responsive to an error signal as indicated by the recitations of Claim 14 reproduced in part below:

> generating a first clock signal responsive to an error signal;
> generating a second clock signal responsive to the error signal;
> ... (emphasis added)

Independent Claim 19 is directed to a system for distributing a clock signal that comprises both a means for generating a first clock signal and a means for generating a second clock signal. Both the means for generating the first clock signal and the means for generating the second clock signal are responsive to an error signal

as indicated by the recitations of Claim 19 reproduced in part below:

> means for generating a first clock signal responsive to an error signal;
> means for generating a second clock signal responsive to the error signal;
> ... (emphasis added)

Thus, independent Claims 1, 14, and 19 all include recitations that indicate that the first and second clock signals are generated responsive to a common error signal.

Doblar describes a system and method for providing redundant, synchronized clocks in a computer system (Doblar, Abstract) in which a clock board 0 105A and a clock board 1 105B are used. Doblar explains that one of the clock boards 0 and 1 (105A and 105B) is used to generate a master clock signal and the other of the clock boards 0 and 1 is used to generate a slave clock signal. If the master clock board were to fail, then the slave clock board may take over to generate the master clock signal. (Doblar, col. 3, lines 39 - 46). Referring to FIG. 2, Doblar further explains that, for example, if clock board 0 is the master board, then the output of the filter 215A, which generates a feedback signal based on a phase difference between the output clock signals of the clock boards 0 and 1, is not provided to the voltage controlled oscillator 220A. Instead, a constant voltage is used to drive the voltage controlled oscillator 220A. (Doblar, col. 4, 34 - 40). It is only when the clock board 0 is used to generate the slave clock signal that the output of the filter 215A is provided to the voltage controlled oscillator 220A to generate the output clock signal 106A. (Doblar, col. 4, lines 41 - 42; *see also*, col. 4,line 58 - col. 5, line 3).

Thus, in sharp contrast to the recitations of independent Claims 1, 14, and 19 which state that both the first and second clock signals are generated responsive to a common error signal, Doblar describes a system in which the slave clock signal is generated responsive to an error signal, which is based on a phase difference between the master clock signal and the slave clock signal, but the master clock signal is not generated responsive to the same error signal that is used to generate the slave clock signal. Rather, the master clock signal is generated responsive to a constant voltage used to drive a voltage-controlled oscillator as discussed above.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that independent Claims 1, 14, and 19 are patentable over the cited reference and that Claims 2 - 7, 15 - 18, and 20 - 24 are patentable at least per the patentability of independent Claims 1, 14, and 19.

Independent Claim 8 is Patentable

Independent Claim 8 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Doblar. Independent Claim 8 is directed to a clock distribution circuit that comprises a plurality of clock circuits that are responsive to respective ones of a plurality of error signals that are generated by respective ones of a plurality of phase detector circuits that directly connect respective ones of the plurality of clock circuits to one or more other ones of the clock circuits as indicated by the recitations of Claim 8 reproduced in part below:

> ...
> a plurality of clock circuits, respective ones of the plurality of clock circuits being directly connected to at least one other of the plurality of clock circuits by respective ones of the plurality of phase detector circuits, respective ones of the plurality of phase detector circuits being configured to generate respective ones of a plurality of error signals responsive to respective ones of a plurality of clock signals generated by the respective ones of the plurality of clock circuits that are directly connected thereby, the respective ones of the plurality of clock circuits being configured to generate respective ones of the plurality of clock signals responsive to respective ones of the plurality of error signals that are generated by the respective ones of the plurality of phase detector circuits that directly connect the respective ones of the plurality of clock circuits to the at least one other of the plurality of clock circuits. (emphasis added)

According to Claim 8, the clock circuits generate the clock signals responsive to error signals generated by phase detectors that connect the clock circuits.

The Office Action states that independent Claim 8 is rejected under the same rationale used to reject Claims 1 and 2. (Office Action, page 5). Applicants respectfully submit that Claim 8 is patentable over Doblar for at least the same reasons discussed above with respect to independent Claims 1, 14, and 19. That is, Doblar does not disclose, teach, or suggest

generating clock signals via respective clock circuits responsive to an error signal that is generated by a phase detector that connects the clock circuits. Instead, Doblar describes a system in which a slave clock signal is generated responsive to an error signal, which is based on a phase difference between the slave clock signal and a master clock signal, but the master clock signal is not generated responsive to this error signal. Instead, the master clock signal is generated responsive to a constant voltage that is used to drive a voltage-controlled oscillator as discussed above.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that independent Claim 8 is patentable over the cited reference and that Claims 9 - 13 are patentable at least per the patentability of independent Claim 8.

Independent Claims 25 and 26 Are Patentable

Independent Claims 25 and 26 stand rejected under 35 U.S.C. §103(a) as being obvious over Doblar in view of U. S. Patent No. 6,822,925 to Van De Graaff (hereinafter "Van De Graaff"). Applicants respectfully submit that Van de Graaff does not qualify as prior art against the present application. Van de Graaff has a filing date of September 23, 2003 and claims priority back to an application filed May 25, 2001. The present application was filed July 31, 2001 and claims priority to a provisional application filed July 31, 2000. Thus, even assuming that the Van de Graaff parent application filed May 25, 2001 includes the same disclosure as Van De Graaff patent no. 6,822,925, Applicants' claim of priority to the provisional application filed July 31, 2000 removes Van De Graaff patent no. 6,822,925 along with all of the Van De Graaff parent patents as prior art.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that independent Claims 25 and 26 are patentable over Doblar and Van De Graaff.

Various Dependent Claims are Separately Patentable

With regard to Claim 2, this claim includes all the recitations of independent Claim 1 and is, therefore, patentable over the cited reference for at least the reasons stated above. Applicants further submit, however, that Claim 2 is separately patentable because Doblar

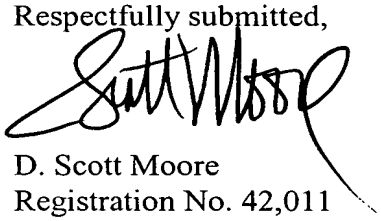
does not disclose or suggest the recitation "wherein the first clock circuit is further configured to generate the first clock signal responsive to the first and second error signals." Applicants respectfully submit that Doblar contains no disclosure or suggestion of generating a clock signal based on multiple error signals. Applicants further submit that Claim 16 is separately patentable for similar reasons.

With regard to Claim 4, this claim includes all the recitations of independent Claim 1 and is, therefore, patentable over the cited reference for at least the reasons stated above. Applicants further submit, however, that Claim 4 is separately patentable because there would be no motivation to modify Doblar to include "a summation circuit that is configured to add the first and the second error signals..." as recited in Claim 4. Applicants submit that there would be no motivation to modify Doblar to include a summation circuit for adding multiple error signals because, as discussed above with respect to Claim 2, Doblar does not disclose or suggest generating a clock signal responsive to a summation of multiple error signals. Applicants further submit that Claim 10, 17, and 22 are separately patentable for similar reasons.

CONCLUSION

In light of the above amendments and remarks, Applicants respectfully submit that the above-entitled application is now in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

Respectfully submitted,



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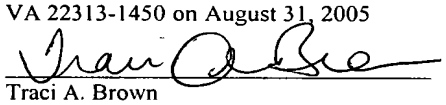

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